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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/612,260	07/07/2000	Guy M. Cohen	YOR9-2000-0174	7116

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EXAMINER
KANG, DONGHEE

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 09/20/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Offic Action Summary	Application No.	Applicant(s)	
	09/612,260	COHEN ET AL.	
	Examiner	Art Unit	
	Donghee Kang	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 July 2002* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20 and 44-51* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20 and 44-51* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Acknowledgment

1. Applicant's amendment and Response to Paper No.17 has been entered and made of Record. New claims 44-51 have been added. Hence, claims **1-20 & 44-51** are pending in this application.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims **1, 4, 7-10 & 44-47** are rejected under 35 U.S.C. 102(b) as being anticipated by Yamanaka (US 5,834,797).

Regarding claims **1 & 46**, Yamanaka discloses a transistor comprising (Figs.8A & 8B):

a channel region (4); a first gate (G2) on top of said channel region; a second gate (G1) below said channel region; and an isolation layer (3) below said second gate, wherein said first gate and second gate are electrically separated from each other and

said first gate and second gate positions said first gate above and aligned with said second gate. See also Col.12, line 41 – Col.14, line 4.

Although Yamanaka does not explicitly teach the first and second gates are self-aligned, "self aligned" is a product-by-process limitation. The product-by-process claims are given no patentable weight. A product-by-process claim directed to the product per

se, no matter how actually made, In re Hirao, 190 USPQ 15 at 17 (footnote 3). See In re Fessman, 180 USPQ 324, 326 (CCPA 1974); In re Marosi et al., 218 USPQ 289, 292 (Fed.Cir.1983); and particularly In re Thrope, 227 USPQ 964, 966 (Fed. Cir. 1985), all of which make it clear that it is the patentability in a "product-by-process" claim, and not the patentability of the process step, which must be determined in a "product-by-process" claim, and not the patentability of the process. See also MPEP 2113. Moreover, an old and obvious product produced by a new method is not a patentable product, whether claimed in "product by process" claims or not.

Regarding claim **4**, Yamanaka discloses the transistor further comprising a first gate dielectric (51 & 52) below said first gate (G2) and a second gate dielectric (30) above said second gate (G1).

Regarding claim **7**, Yamanaka discloses the first gate comprises a different thickness than said second gate.

Regarding claim **8**, Yamanaka discloses said first gate, said second gate and said channel region form a planarized structure.

Regarding claim **9**, Yamanaka discloses said first gate dielectric comprises a different material than said second gate dielectric.

Regarding claim **10**, Yamanaka discloses said first gate dielectric comprises a different thickness than second gate dielectric.

Regarding claim **44**, Yamanaka discloses a transistor comprising (Figs.8A & 8B):

a channel region (4); a first gate (G2) on top of said channel region; a second gate (G1) below said channel region; and an isolation layer (3) below said second gate;

source and drain regions laterally adjacent said channel region, wherein said source and drain regions do not horizontally overlap said first gate or second gate, and

wherein said first gate and said second gate are electrically separated from each other. See also Col.12, line 41 – Col.14, line 4.

Although Yamanaka does not explicitly teach the source and drain regions are self-aligned with the first and second gates, this limitation is product-by-process limitation. The product-by-process claims are given no patentable weight. See the rejection of claim 1 explained above.

Regarding claim **45**, Yamanaka discloses a transistor comprising (Figs.8A & 8B):

a channel region (4); a first gate (G2) on top of said channel region; a second gate (G1) below said channel region; and an isolation layer (3) below said second gate; source and drain regions laterally adjacent said channel region, said first gate, and said second gate, and

wherein said first gate and said second gate are electrically separated from each other. See also Col.12, line 41 – Col.14, line 4.

Regarding claim **47**, Yamanaka discloses the transistor further comprising (Figs. 8a & 8B):

source and drain regions laterally adjacent said channel region, said first gate, and said second gate; and source and drain dielectric between said source and drain regions and said first gate and said second gate,

wherein a thickness and material selection of said first gate dielectric and said second gate dielectric is independent of said source and drain dielectrics.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims **2-3** are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamanaka.

Yamanaka teaches substantially the entire claimed structure, applied to claim 1 as explained above, except that the first gate comprises a different doping concentration and doping species than said second gate.

It is, however, well known in the art to select the concentration of gate electrode to adjust a threshold voltage in the transistor. If the first gate electrode has a lower concentration than the second gate electrode, a threshold voltage of the first gate is lower than that of the second gate. Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have formed Yamanaka's "first and second gate" having a different concentration, since the different concentration of gate electrode provides the different threshold voltage in device.

6. Claim **5** is rejected under 35 U.S.C. 103(a) as being unpatentable over Yamanaka in view of Uesugi et al. (US 5,708,286).

Yamanaka applies to claims 1 above.

Although Yamanaka fails to teach first conductive contact of first gate and second conductive contact of second gate are coplanar, Uesugi et al teaches in Fig.1 & Col.7, lines 42-46 the first conductive contact (80) of first gate (60) and second conductive contact (90) of second gate (30) are coplanar. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teaching of Uesugi with Yamanaka's device in order to reduce the manufacturing processing.

7. Claims **6,11-16, 18-20, & 48-51** are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamanaka in view of Pfiester (US 5,166,084).

Regarding claims **6 & 11**, Yamanaka discloses a semiconductor chip having at least on transistor, said transistor comprising (Figs. 8a & 8B):

a channel region (4); a first gate (G2) on top of said channel region; a second gate (G1) below said channel region; and an isolation layer (3) below said second gate. See also Col.12, line 41 – Col.14, line 4.

Although Yamanaka does not explicitly teach the first and second gates are self-aligned, "self-aligned" is a product-by-process limitation. The product-by-process claims are given no patentable weight. See the rejection of claim 1 explained above.

Although Yamanaka does not explicitly teach the first gate comprises a different material than said second gate. However, Pfiester teaches in Fig.4 the first gate electrode (24) comprise a different material than said second gate electrode (26). Thus, it would have been obvious to one having ordinary skill in the art at the time the

invention was made to incorporate the teaching of Pfiester into Yamanaka's device, since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. *In re Leshin*, 125 USPQ 416.

Regarding claims **12-13**, neither Yamanaka nor Pfiester teaches the first gate comprises a different doping concentration and doping species than said second gate. It would have been obvious to have the first gate comprises a different doping concentration and doping species than the second gate for the same reason as given in the rejection of claim 2.

Regarding claim **14**, Yamanaka as modified by Pfiester discloses the transistor further comprising a first gate dielectric (51 & 52) below said first gate (G2) and a second gate dielectric (30) above said second gate (G1).

Regarding claim **15**, Yamanaka as modified by Pfiester discloses said first gate dielectric comprises a different material than said second gate dielectric.

Regarding claim **16**, Yamanaka as modified by Pfiester discloses said first gate dielectric comprises a different thickness than second gate dielectric.

Regarding claim **18**, Yamanaka as modified by Pfiester discloses said first gate and said second gate are electrically separated.

Regarding claim **19**, Yamanaka as modified by Pfiester discloses the first gate and said second gate have different thickness.

Regarding claim **20**, Yamanaka as modified by Pfiester discloses said first gate, said second gate and said channel region form a planarized structure.

Regarding claims **48 & 49**, Yamanaka as modified by Pfiester teaches the semiconductor chip further comprising source and drain regions laterally adjacent said channel region, wherein said source and drain regions do not horizontally overlap said first or said second gate, and

said first gate and said second gate positions said first gate above and aligned with said second gate.

Although Yamanaka does not explicitly teach the source and drain regions are self-aligned with said first gate and said second gate, this limitation is product-by-process limitation. The product-by-process claims are given no patentable weight. See the rejection of claim 1 explained above.

Regarding claim **50**, Yamanaka as modified by Pfiester teaches the semiconductor chip further comprising source and drain regions laterally adjacent said channel region, said first gate, and said second gate.

Regarding claim **51**, Yamanaka as modified by Pfiester discloses the transistor further comprising (Figs. 8a & 8B):

source and drain regions laterally adjacent said channel region, said first gate, and said second gate; and source and drain dielectric between said source and drain regions and said first gate and said second gate,

wherein a thickness and material selection of said first gate dielectric and said second gate dielectric is independent of said source and drain dielectrics.

8. Claim **17** is rejected under 35 U.S.C. 103(a) as being unpatentable over Yamanaka in view of Pfiester and further in view of Uesugi et al. (US 5,708,286).

Yamanaka as modified by Pfiester applies to claims 11 above.

Although Yamanaka as modified by Pfiester fails to teach first conductive contact of first gate and second conductive contact of second gate are coplanar, Uesugi et al teaches in Fig.1 & Col.7, lines 42-46 the first conductive contact (80) of first gate (60) and second conductive contact (90) of second gate (30) are coplanar. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teaching of Uesugi with Yamanaka's device in order to reduce the manufacturing processing.

Response to Arguments

9. Applicant's arguments with respect to claims 1-20 & 44-51 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Donghee Kang whose telephone number is 703-305-9147. The examiner can normally be reached on Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on 703-308-2772. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722 for regular communications and 703-308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

Donghee Kang, Ph.D.
September 10, 2002

Steven Loke
Primary Examiner